AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended): A semiconductor device having a multiple layer wiring structure that is provided with two or more metal layers and having a stack VIA portion for connecting in a connection area a connection metal layer and a layer to be connected that is removed from the connection metal layer with one or more intermediate metal layers, comprising:

two or more partitioned intermediate metal layers that are partitioned inside the connection area; and

an intermediate metal layer wiring area for an ordinary wiring that is sandwiched by the partitioned intermediate metal layers,

wherein the intermediate metal layer wiring area is not connected with the stack VIA.

Claim 2 (previously presented): The semiconductor device according to claim 1, wherein the connection metal layer and the layer to be connected intersect in the connection area.

Claim 3 (original): The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the intermediate metal layer wiring area is formed in a priority wiring direction in the intermediate metal layer.

Claim 4 (original): The semiconductor device having a multiple layer wiring structure according to claim 1, wherein appropriate partitioned areas of the intermediate metal layers are secured and the intermediate metal layer wiring areas are formed by deleting appropriate interlayer connection portions that connect the metal layers forming the stack VIA portion.

Claim 5 (original): The semiconductor device having a multiple layer wiring structure according to claim 4, wherein the interlayer connection portions are arranged in an array configuration that matches wiring tracks running in the priority wiring direction in the intermediate metal layers connected to the interlayer connection portions, and are deleted where appropriate in row units running in the priority wiring direction.

Claim 6 (previously presented): The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the partitioned intermediate metal layers are formed in accordance with minimum design rules in a direction that is orthogonal to the priority wiring direction of the intermediate metal layer.

Claim 7 (original): The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the layer to be connected is a metal layer.

Claim 8 (original): The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the layer to be connected is a non-metal layer.

Claim 9 (original): The semiconductor device having a multiple layer wiring structure according to claim 8, wherein the non-metal layer is a polycrystalline silicon layer.

Claim 10 (original): The semiconductor device having a multiple layer wiring structure according to claim 8, wherein the non-metal layer is a diffusion layer.

Claims 11-18 (canceled).

Claim 19 (currently amended): A semiconductor device having a multiple layer wiring and a stack VIA, comprising:

a connection metal layer;

a layer to be connected with the connection metal layer; and

one or more intermediate layers, provided between the connection metal layer and the layer to be connected, partitioned into two or more partitioned intermediate layers,

wherein the partitioned intermediate metal layers comprise:

at least one intermediate metal layer having a stack VIA; and

at least one intermediate metal layer wiring area ~~where a wire can be passed through~~ which is not connected with the stack VIA but used for wiring.

Claim 20 (currently amended): A semiconductor device having a multiple layer wiring and a stack VIA, wherein the semiconductor device is generated by the method provided with an automatic wiring design program for performing wiring design automatically using the wiring method, the wiring method comprising:

a step of determining a connection metal layer and a layer to be connected with the connection metal layer that is removed from the connection metal layer with one or more intermediate metal layers;

a step of connecting the connection metal layer and the layer to be connected via a partitioned intermediate metal layer having a stack VIA,

wherein the one or more intermediate layers are partitioned into at least one partitioned intermediate metal layer and at least one intermediate metal layer wiring area not connected with the stack VIA but used for wiring.

Claim 21 (currently amended): A semiconductor device having multiple layer wiring and a stack VIA, wherein the semiconductor device is generated by the method provided with an

automatically wiring design program for performing wiring design automatically using the wiring method, and when connecting in a connection area a connection metal layer and a layer to be connected that is removed from the connection metal layer with one or more intermediate metal layers, the intermediate metal layers are partitioned within the connection area, and an area sandwiched by the ~~partitioned intermediate metal layers~~ connection areas is formed as an intermediate metal layer wiring area, which is not connected with the stack VIA but is used for wiring.

Claim 22 (previously presented): The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the intermediate metal layer wiring area is formed in a priority wiring direction in the intermediate metal layer.

Claim 23 (previously presented): The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein appropriate partitioned areas of the intermediate metal layers are secured and the intermediate metal layer wiring areas are formed by deleting appropriate interlayer connection portions that connect the metal layers forming the stack VIA portion.

Claim 24 (previously presented): The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the interlayer connection portions are

arranged in an array configuration that matches wiring tracks running in the priority wiring direction in the intermediate metal layers connected to the interlayer connection portions, and are detected where appropriate in row units running in the priority wiring direction.

Claim 25 (previously presented): The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the portioned intermediated metal layers are formed in accordance with minimum design rules in a direction that is orthogonal to the priority wiring direction of the intermediate metal layer.

Claim 26 (previously presented): The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the layer to be connected is a metal layer.

Claim 27 (previously presented): The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the layer to be connected is a non-metal layer.

Claim 28 (previously presented): The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the non-metal layer is polycrystalline silicon layer.

Claim 29 (previously presented): The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the non-metal layer is a diffusion layer.

Claim 30 (currently amended): A semiconductor device having a multiple layer wiring and a stack VIA comprising:

a connection metal layer;

a layer to be connected with the connection metal layer;

one or more intermediate metal layers to be provided between the connection metal layer and the layer to be connected; and

a connection area for connecting the connection metal layer and the layer to be connected,

wherein the intermediate metal layer in the connection area is partitioned into two or more partitioned intermediate metal layers, ~~at least one partitioned intermediate metal layer for wiring~~ the partitioned intermediate metal layer which is not connected with the stack VIA is used for wiring.